Hi can you send out a version that supports kc705, I really need your help. #115

Open **uk0** opened this issue on Dec 28, 2022 · 5 comments

uk0 commented on Dec 28, 2022

No description provided.

ufrisk commented on Dec 28, 2022

Hi,

Like I mentioned before I don't have a KC705 at hand. I'm also really really hesitant in creating a firmware for a device I won't be able to test it on. Worst case if it's not working out-of-the-box I'll be sitting with endless support questions eating up whatever little time I might have. Thanks for understanding.

If you study the AC701 project you may be able to pull it off yourself though. Changes should hopefully be mostly around editing the constaints file with the new pins.

uk0 commented on Dec 28, 2022

I modified the constaints and re-modified the voltage 2.5-> 1.8, passed the compilation, and generated the bin flash successfully, but it cannot be started. Now I guess what should be the cause of the reset.

ufrisk commented on Dec 30, 2022

It's just very hard for me to tell what's wrong remotely without having my own KC705 to test on :(

You'll have to try to do some debugging to see what may be causing the issues.

FreshPizza commented 12 hours ago • edited

I was curious so I ended up implementing this for a KC705 I had available. There's several revisions of the board. I have the 1.1/1.2 revision, and some of these boards may have different QSPI ICs (so flashing may fail, but it should print the detected part on the board).

I also couldn't quite get 4.11 working on the KC705 or AC701 either, not sure why, but didn't feel like troubleshooting that so I just used version 4.10

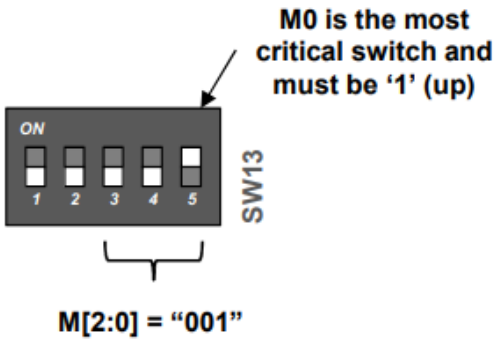
```
Memory Dump: Initializing ... Done.
 Current Action: Dumping Memory
 Access Mode:    Normal
 Progress:       19424 / 19424 (100%)
 Speed:          223 MB/s
 Address:        0x0000000100000000
 Pages read:     4181664 / 4972544 (84%)
 Pages failed:   790880 (15%)
Memory Dump: Successful.

C:\Users\      \Documents\Desktop\pcileech-4.15>pcileech dump -device FPGA

Memory Dump: Initializing ... Done.
 Current Action: Dumping Memory
 Access Mode:    Normal
 Progress:       19424 / 19424 (100%)
 Speed:          223 MB/s
 Address:        0x0000000100000000
 Pages read:     4181664 / 4972544 (84%)
 Pages failed:   790880 (15%)
Memory Dump: Successful.
```

DIP switch for SPI:

DIP switches SW13 must
be set to Master SPI Mode.



Memory Configuration Device (again, you may have a different device on your board):

```
mt25ql128-spi-x1_x2_x4
```

XDC for pcileech-FPGA **4.10**

```
##################################################
####  HPC definition, default FMC connector  ####
##################################################

# FMC_HPC_LA10_N
set_property PACKAGE_PIN C30 [get_ports ft601_rst_n]
# FMC_HPC_LA00_CC_P
set_property PACKAGE_PIN C25 [get_ports ft601_oe_n]
# FMC_HPC_LA00_CC_N
set_property PACKAGE_PIN B25 [get_ports ft601_rd_n]
# FMC_HPC_LA08_P
set_property PACKAGE_PIN E29 [get_ports ft601_wr_n]
# FMC_HPC_LA07_P
set_property PACKAGE_PIN E28 [get_ports ft601_rxf_n]
# FMC_HPC_LA07_N
```

```
# FMC_HPC_LA15_N
set_property PACKAGE_PIN B24 [get_ports {ft601_be[0]}]
# FMC_HPC_LA15_P
set_property PACKAGE_PIN C24 [get_ports {ft601_be[1]}]
# FMC_HPC_LA09_N
set_property PACKAGE_PIN A30 [get_ports {ft601_be[2]}]
# FMC_HPC_LA09_P
set_property PACKAGE_PIN B30 [get_ports {ft601_be[3]}]
# FMC_HPC_LA32_N
set_property PACKAGE_PIN C21 [get_ports {ft601_data[0]}]
# FMC_HPC_LA33_N
set_property PACKAGE_PIN H22 [get_ports {ft601_data[1]}]
# FMC_HPC_LA32_P
set_property PACKAGE_PIN D21 [get_ports {ft601_data[2]}]
# FMC_HPC_LA33_P
set_property PACKAGE_PIN H21 [get_ports {ft601_data[3]}]
# FMC_HPC_LA30_N
set_property PACKAGE_PIN C22 [get_ports {ft601_data[4]}]
# FMC_HPC_LA31_N
set_property PACKAGE_PIN F22 [get_ports {ft601_data[5]}]
# FMC_HPC_LA30_P
set_property PACKAGE_PIN D22 [get_ports {ft601_data[6]}]
# FMC_HPC_LA31_P
set_property PACKAGE_PIN G22 [get_ports {ft601_data[7]}]
# FMC_HPC_LA28_N
set_property PACKAGE_PIN C16 [get_ports {ft601_data[8]}]
# FMC_HPC_LA29_N
set_property PACKAGE_PIN B17 [get_ports {ft601_data[9]}]
# FMC_HPC_LA28_P
set_property PACKAGE_PIN D16 [get_ports {ft601_data[10]}]
# FMC_HPC_LA29_P
set_property PACKAGE_PIN C17 [get_ports {ft601_data[11]}]
# FMC_HPC_LA24_N
set_property PACKAGE_PIN A17 [get_ports {ft601_data[12]}]
# FMC_HPC_LA25_N
set_property PACKAGE_PIN F17 [get_ports {ft601_data[13]}]
# FMC_HPC_LA24_P
set_property PACKAGE_PIN A16 [get_ports {ft601_data[14]}]
# FMC_HPC_LA25_P
set_property PACKAGE_PIN G17 [get_ports {ft601_data[15]}]
# FMC_HPC_LA27_N
set_property PACKAGE_PIN B19 [get_ports {ft601_data[16]}]
# FMC_HPC_LA26_N
set_property PACKAGE_PIN A18 [get_ports {ft601_data[17]}]
# FMC_HPC_LA27_P
set_property PACKAGE_PIN C19 [get_ports {ft601_data[18]}]
# FMC_HPC_LA26_P
set_property PACKAGE_PIN B18 [get_ports {ft601_data[19]}]
# FMC_HPC_LA21_N
set_property PACKAGE_PIN A21 [get_ports {ft601_data[20]}]
# FMC_HPC_LA22_N
set_property PACKAGE_PIN B20 [get_ports {ft601_data[21]}]
# FMC_HPC_LA21_P
set_property PACKAGE_PIN A20 [get_ports {ft601_data[22]}]
# FMC_HPC_LA22_P
set_property PACKAGE_PIN C20 [get_ports {ft601_data[23]}]
# FMC_HPC_LA23_N
set_property PACKAGE_PIN A22 [get_ports {ft601_data[24]}]
# FMC_HPC_LA23_P
set_property PACKAGE_PIN B22 [get_ports {ft601_data[25]}]
# FMC_HPC_LA19_N
set_property PACKAGE_PIN F18 [get_ports {ft601_data[26]}]
# FMC_HPC_LA19_P
set_property PACKAGE_PIN G18 [get_ports {ft601_data[27]}]
# FMC_HPC_LA20_N
```

```
# FMC_HPC_LA17_CC_N
set_property PACKAGE_PIN E20 [get_ports {ft601_data[30]}]
# FMC_HPC_LA17_CC_P
set_property PACKAGE_PIN F20 [get_ports {ft601_data[31]}]
# FT601 CLK -- FMC_HPC_LA18_CC_P
set_property PACKAGE_PIN F21 [get_ports ft601_clk]

#####################################################
####  LPC definition in case someone wants this  ####
####  Uncomment below and comment above to use   ####
#####################################################

##FMC_LPC_LA00_CC_N
#set_property PACKAGE_PIN AE24 [get_ports ft601_rd_n]
##FMC_LPC_LA00_CC_P
#set_property PACKAGE_PIN AD23 [get_ports ft601_oe_n]
##FMC_LPC_LA07_N
#set_property PACKAGE_PIN AH25 [get_ports ft601_txe_n]
##FMC_LPC_LA07_P
#set_property PACKAGE_PIN AG25 [get_ports ft601_rxf_n]
##FMC_LPC_LA08_N
#set_property PACKAGE_PIN AJ23 [get_ports ft601_siwu_n]
##FMC_LPC_LA08_P
#set_property PACKAGE_PIN AJ22 [get_ports ft601_wr_n]
##FMC_LPC_LA09_N
#set_property PACKAGE_PIN AK24 [get_ports {ft601_be[2]}]
##FMC_LPC_LA09_P
#set_property PACKAGE_PIN AK23 [get_ports {ft601_be[3]}]
##FMC_LPC_LA10_N
#set_property PACKAGE_PIN AK25 [get_ports ft601_rst_n]
##FMC_LPC_LA15_N
#set_property PACKAGE_PIN AD24 [get_ports {ft601_be[0]}]
##FMC_LPC_LA15_P
#set_property PACKAGE_PIN AC24 [get_ports {ft601_be[1]}]
##FMC_LPC_LA17_CC_N
#set_property PACKAGE_PIN AC27 [get_ports {ft601_data[30]}]
##FMC_LPC_LA17_CC_P
#set_property PACKAGE_PIN AB27 [get_ports {ft601_data[31]}]
##FMC_LPC_LA19_N
#set_property PACKAGE_PIN AK26 [get_ports {ft601_data[26]}]
##FMC_LPC_LA19_P
#set_property PACKAGE_PIN AJ26 [get_ports {ft601_data[27]}]
##FMC_LPC_LA20_N
#set_property PACKAGE_PIN AF27 [get_ports {ft601_data[28]}]
##FMC_LPC_LA20_P
#set_property PACKAGE_PIN AF26 [get_ports {ft601_data[29]}]
##FMC_LPC_LA21_N
#set_property PACKAGE_PIN AG28 [get_ports {ft601_data[20]}]
##FMC_LPC_LA21_P
#set_property PACKAGE_PIN AG27 [get_ports {ft601_data[22]}]
##FMC_LPC_LA22_N
#set_property PACKAGE_PIN AK28 [get_ports {ft601_data[21]}]
##FMC_LPC_LA22_P
#set_property PACKAGE_PIN AJ27 [get_ports {ft601_data[23]}]
##FMC_LPC_LA23_N
#set_property PACKAGE_PIN AH27 [get_ports {ft601_data[24]}]
##FMC_LPC_LA23_P
#set_property PACKAGE_PIN AH26 [get_ports {ft601_data[25]}]
##FMC_LPC_LA24_N
#set_property PACKAGE_PIN AH30 [get_ports {ft601_data[12]}]
##FMC_LPC_LA24_P
#set_property PACKAGE_PIN AG30 [get_ports {ft601_data[14]}]
##FMC_LPC_LA25_N
#set_property PACKAGE_PIN AD26 [get_ports {ft601_data[13]}]
##FMC_LPC_LA25_P
```

```
##FMC_LPC_LA26_P
#set_property PACKAGE_PIN AK29 [get_ports {ft601_data[19]}]
##FMC_LPC_LA27_N
#set_property PACKAGE_PIN AJ29 [get_ports {ft601_data[16]}]
##FMC_LPC_LA27_P
#set_property PACKAGE_PIN AJ28 [get_ports {ft601_data[18]}]
##FMC_LPC_LA28_N
#set_property PACKAGE_PIN AF30 [get_ports {ft601_data[8]}]
##FMC_LPC_LA28_P
#set_property PACKAGE_PIN AE30 [get_ports {ft601_data[10]}]
##FMC_LPC_LA29_N
#set_property PACKAGE_PIN AF28 [get_ports {ft601_data[9]}]
##FMC_LPC_LA29_P
#set_property PACKAGE_PIN AE28 [get_ports {ft601_data[11]}]
##FMC_LPC_LA30_N
#set_property PACKAGE_PIN AB30 [get_ports {ft601_data[4]}]
##FMC_LPC_LA30_P
#set_property PACKAGE_PIN AB29 [get_ports {ft601_data[6]}]
##FMC_LPC_LA31_N
#set_property PACKAGE_PIN AE29 [get_ports {ft601_data[5]}]
##FMC_LPC_LA31_P
#set_property PACKAGE_PIN AD29 [get_ports {ft601_data[7]}]
##FMC_LPC_LA32_N
#set_property PACKAGE_PIN AA30 [get_ports {ft601_data[0]}]
##FMC_LPC_LA32_P
#set_property PACKAGE_PIN Y30 [get_ports {ft601_data[2]}]
##FMC_LPC_LA33_N
#set_property PACKAGE_PIN AC30 [get_ports {ft601_data[1]}]
##FMC_LPC_LA33_P
#set_property PACKAGE_PIN AC29 [get_ports {ft601_data[3]}]
## FT601 CLK -- FMC_LPC_LA18_CC_P
#set_property PACKAGE_PIN AD27 [get_ports ft601_clk]

set_property IOSTANDARD LVCMOS18 [get_ports {ft601_txe_n ft601_rxf_n}]
set_property IOSTANDARD LVCMOS18 [get_ports {{ft601_be[*]} {ft601_data[*]}}]
set_property IOSTANDARD LVCMOS18 [get_ports {ft601_wr_n ft601_rd_n ft601_oe_n ft601_siwu_n
ft601_rst_n}]
set_property SLEW FAST [get_ports {{ft601_be[*]} {ft601_data[*]}}]
set_property SLEW FAST [get_ports {ft601_wr_n ft601_rd_n ft601_oe_n ft601_siwu_n ft601_rst_n}]

set_property PACKAGE_PIN AB8 [get_ports gpio_led[0]]
set_property IOSTANDARD LVCMOS15 [get_ports gpio_led[0]]
set_property PACKAGE_PIN AA8 [get_ports gpio_led[1]]
set_property IOSTANDARD LVCMOS15 [get_ports gpio_led[1]]
set_property PACKAGE_PIN AC9 [get_ports gpio_led[2]]
set_property IOSTANDARD LVCMOS15 [get_ports gpio_led[2]]
set_property PACKAGE_PIN AA12 [get_ports gpio_sw_north]
set_property IOSTANDARD LVCMOS15 [get_ports gpio_sw_north]
set_property PACKAGE_PIN AB12 [get_ports gpio_sw_south]
set_property IOSTANDARD LVCMOS15 [get_ports gpio_sw_south]

# SYSCLK
set_property PACKAGE_PIN AD12 [get_ports sysclk_p]
set_property PACKAGE_PIN AD11 [get_ports sysclk_n]
set_property IOSTANDARD LVDS [get_ports sysclk_p]
set_property IOSTANDARD LVDS [get_ports sysclk_n]


set_property IOSTANDARD LVCMOS18 [get_ports ft601_clk]
create_clock -period 10.000 -name net_ft601_clk -waveform {0.000 5.000} [get_ports ft601_clk]

set_input_delay -clock [get_clocks net_ft601_clk] -min 6.5 [get_ports {ft601_data[*]}]
set_input_delay -clock [get_clocks net_ft601_clk] -max 7.0 [get_ports {ft601_data[*]}]
set_input_delay -clock [get_clocks net_ft601_clk] -min 6.5 [get_ports ft601_rxf_n]
set_input_delay -clock [get_clocks net_ft601_clk] -max 7.0 [get_ports ft601_rxf_n]
```

```
set_output_delay -clock [get_clocks net_ft601_clk] -max 1.0 [get_ports {ft601_wr_n ft601_rd_n
ft601_oe_n}]
set_output_delay -clock [get_clocks net_ft601_clk] -min 4.8 [get_ports {ft601_wr_n ft601_rd_n
ft601_oe_n}]
set_output_delay -clock [get_clocks net_ft601_clk] -max 1.0 [get_ports {{ft601_be[*]}
{ft601_data[*]}}]
set_output_delay -clock [get_clocks net_ft601_clk] -min 4.8 [get_ports {{ft601_be[*]}
{ft601_data[*]}}]

set_property IOB TRUE [get_cells i_pcileech_com/i_pcileech_ft601/FT601_OE_N_reg]
set_property IOB TRUE [get_cells i_pcileech_com/i_pcileech_ft601/FT601_RD_N_reg]
set_property IOB TRUE [get_cells i_pcileech_com/i_pcileech_ft601/FT601_WR_N_reg]
set_property IOB TRUE [get_cells i_pcileech_com/i_pcileech_ft601/txo_dout_reg[*]]

set_multicycle_path 2 -from [get_pins i_pcileech_com/i_pcileech_ft601/oe_reg/C] -to [get_ports
{{ft601_be[*]} {ft601_data[*]}}]
set_false_path -from [get_pins {tickcount64_reg[*]/C}]
set_false_path -from [get_pins {i_pcileech_fifo/_pcie_core_config_reg[*]/C}]
set_false_path -from [get_pins i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/user_lnk_up_int_reg/C] -to
[get_pins {i_pcileech_fifo/_cmd_tx_din_reg[16]/D}]
set_false_path -from [get_pins i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/user_reset_out_reg/C]

#PCIe signals
set_property PACKAGE_PIN G25 [get_ports pcie_perst_n]
set_property PACKAGE_PIN F23 [get_ports pcie_wake_n]
set_property IOSTANDARD LVCMOS18 [get_ports pcie_perst_n]
set_property IOSTANDARD LVCMOS18 [get_ports pcie_wake_n]

set_property LOC GTXE2_CHANNEL_X0Y7 [get_cells
{i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/gt_top_i/pipe_wrapper_i/pipe_lane[0].gt_wrapper_i/gtx_channe
set_property PACKAGE_PIN L4 [get_ports {pcie_tx_p[0]}]
set_property PACKAGE_PIN M6 [get_ports {pcie_rx_p[0]}]
set_property PACKAGE_PIN L3 [get_ports {pcie_tx_n[0]}]
set_property PACKAGE_PIN M5 [get_ports {pcie_rx_n[0]}]

#set_property LOC GTXE2_CHANNEL_X0Y6 [get_cells
{i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/gt_top_i/pipe_wrapper_i/pipe_lane[1].gt_wrapper_i/gtx_channe
#set_property PACKAGE_PIN M2 [get_ports {pcie_tx_p[1]}]
#set_property PACKAGE_PIN P6 [get_ports {pcie_rx_p[1]}]
#set_property PACKAGE_PIN M1 [get_ports {pcie_tx_n[1]}]
#set_property PACKAGE_PIN P5 [get_ports {pcie_rx_n[1]}]

#set_property LOC GTXE2_CHANNEL_X0Y5 [get_cells
{i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/gt_top_i/pipe_wrapper_i/pipe_lane[2].gt_wrapper_i/gtx_channe
#set_property PACKAGE_PIN N4 [get_ports {pcie_tx_p[2]}]
#set_property PACKAGE_PIN R4 [get_ports {pcie_rx_p[2]}]
#set_property PACKAGE_PIN N3 [get_ports {pcie_tx_n[2]}]
#set_property PACKAGE_PIN R3 [get_ports {pcie_rx_n[2]}]

#set_property LOC GTXE2_CHANNEL_X0Y4 [get_cells
{i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/gt_top_i/pipe_wrapper_i/pipe_lane[3].gt_wrapper_i/gtx_channe
#set_property PACKAGE_PIN P2 [get_ports {pcie_tx_p[3]}]
#set_property PACKAGE_PIN T6 [get_ports {pcie_rx_p[3]}]
#set_property PACKAGE_PIN P1 [get_ports {pcie_tx_n[3]}]
#set_property PACKAGE_PIN T5 [get_ports {pcie_rx_n[3]}]

#set_property LOC GTXE2_CHANNEL_X0Y3 [get_cells
{i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/gt_top_i/pipe_wrapper_i/pipe_lane[4].gt_wrapper_i/gtx_channe
#set_property PACKAGE_PIN T2 [get_ports {pcie_tx_p[4]}]
#set_property PACKAGE_PIN V6 [get_ports {pcie_rx_p[4]}]
#set_property PACKAGE_PIN T1 [get_ports {pcie_tx_n[4]}]
#set_property PACKAGE_PIN V5 [get_ports {pcie_rx_n[4]}]

#set_property LOC GTXE2_CHANNEL_X0Y2 [get_cells
{i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/gt_top_i/pipe_wrapper_i/pipe_lane[5].gt_wrapper_i/gtx_channe
```

```
#set_property PACKAGE_PIN W3 [get_ports {pcie_rx_n[5]}]

#set_property LOC GTXE2_CHANNEL_X0Y1 [get_cells
{i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/gt_top_i/pipe_wrapper_i/pipe_lane[6].gt_wrapper_i/gtx_channe
#set_property PACKAGE_PIN V2 [get_ports {pcie_tx_p[6]}]
#set_property PACKAGE_PIN Y6 [get_ports {pcie_rx_p[6]}]
#set_property PACKAGE_PIN V1 [get_ports {pcie_tx_n[6]}]
#set_property PACKAGE_PIN Y2 [get_ports {pcie_rx_n[6]}]

#set_property LOC GTXE2_CHANNEL_X0Y0 [get_cells
{i_pcileech_pcie_a7/i_pcie_7x_0/inst/inst/gt_top_i/pipe_wrapper_i/pipe_lane[7].gt_wrapper_i/gtx_channe
#set_property PACKAGE_PIN Y2 [get_ports {pcie_tx_p[7]}]
#set_property PACKAGE_PIN AA4 [get_ports {pcie_rx_p[7]}]
#set_property PACKAGE_PIN Y1 [get_ports {pcie_tx_n[7]}]
#set_property PACKAGE_PIN AA3 [get_ports {pcie_rx_n[7]}]

#PCIe clock
set_property PACKAGE_PIN U7 [get_ports pcie_clk_n]
set_property PACKAGE_PIN U8 [get_ports pcie_clk_p]

create_clock -name pcie_refclk_p -period 10.0 [get_nets pcie_clk_p]

set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]

set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property CFGBVS GND [current_design]
```

ufrisk commented 9 hours ago

Thanks for this info 👍

It's a bit worrisome that the AC701 v4.11 isn't working though. I burnt mine some months ago (and since it's kinda pricey I don't feel like paying for a new one) so I kinda compiled in the new changes blindly. Must have missed something...

Assignees

No one assigned

Labels

None yet

Projects

None yet

Milestone

No milestone

Development

No branches or pull requests

3 participants